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**U.S. UTILITY Patent Application**

| PATENT NUMBER and ISSUE DATE |
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| APPL NUM | FILING DATE | CLASS | SUBCLASS | GAU | EXAMINER |
|---|---|---|---|---|---|
| 10077258 | 02/14/2002 | 257 | 324 | 2814 | |

**APPLICANTS: Mo Brian; Chau Duc; yk

**CONTINUING DATA VERIFIED: yes

THIS APPLICATION IS A DIV OF 09/286,168 04/05/1999 yk



** FOREIGN APPLICATIONS VERIFIED: none yk

| PG-PUB | DO NOT PUBLISH ☐ | RESCIND ☐ |
|---|---|---|

| | | |
|---|---|---|
| Foreign priority claimed | ☐ yes ☑ no | ATTORNEY DOCKET NO |
| 35 USC 119 conditions met | ☐ yes ☑ no | 018865-001010US |
| Verified and Acknowledged Examiners's intials | yk | |

TITLE : Method of forming a trench transistor having a superior gate dielectric

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

| NOTICE OF ALLOWANCE MAILED | Assistant Examiner: Jennifer B. Huynh | CLAIMS ALLOWED | |
|---|---|---|---|
| | | Total Claims: 10 | Print Claim for O.G: 1 |
| ISSUE FEE | | DRAWING | |
| Amount Due / Date Paid | | Sheets Drwg.: 5 | Figs.Drwg.: 7 / Print Fig.: 3, 4 |
| ☐ TERMINAL DISCLAIMER | Primary Examiner / PREPARED FOR ISSUE | Application Examiner | |



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(Attached in pocket on right inside flap)